APPLICATION NOTE

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RF Division
Market Management Test+Measurement
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RF Board Connector: Footprint Optimization The Key To Maximize Your Performance.

The continuous demand for higher data rate is pushing the frequency boundary and performance level of Radio Frequency (RF) components used in a test setup. For design validation testing (DVT), test components including RF test assemblies and RF board connectors, must be “electrically transparent” to ensure a reliable characterization of the device under test (DUT). While low frequency / low data rate applications can forgive the use of a generic footprint for RF board connectors, today’s bandwidth to support data rate of 56Gbps and beyond requires an optimized footprint designed and matched to a specific board stackup to ensure best performance in the desired frequency range. Design cycles are getting shorter to respond to the faster pace of innovation of the markets (semiconductor, 5G, automotive ..) and it is tempting to create a symbol in the design library with a default layout. However consequences on performance can be significant often requiring a new design loop which is time consuming and expensive.

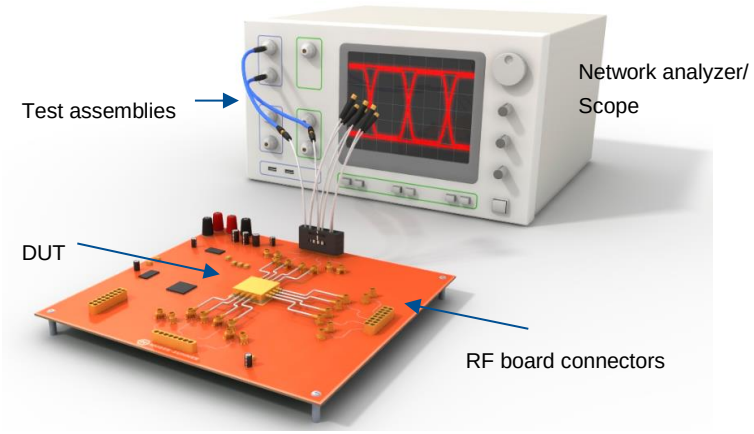
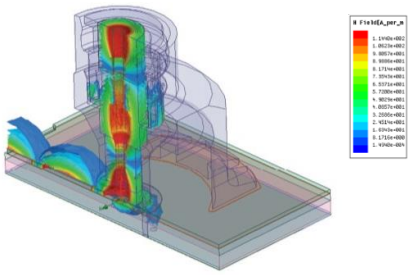


Fig.1: Standard test setup for Design Validation Testing (DVT) with network analyzer and/or scope

Propagation modes

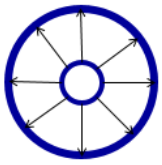
From a signal integrity perspective, the transition to the board is the weakest point as the electromagnetic (EM) field is converted from a coaxial mode (TEM) into a planar mode which depends on the transmission line (typ. microstrip, stripline or grounded coplanar waveguide [GCPW]). The high level of energy must be properly converted in order to avoid reflection and/or resonances which would reduce considerably the performance of the test setup in terms of bandwidth, return loss, insertion loss and impedance matching.



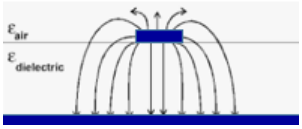
Graph 2: Representation of H-Field transitioning from a coaxial board connector onto a microstrip

The planar propagation mode may differ based on the routing. For instance, the fundamental propagation mode for the most commonly used transmission lines are:

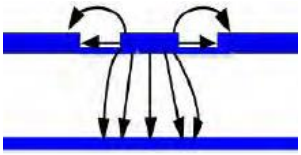
- Coaxial connector: TEM mode
  In the Transverse Electric and Magnetic (TEM) mode, both the electric field and the magnetic field are perpendicular to the direction of propagation.
  E-field representation:



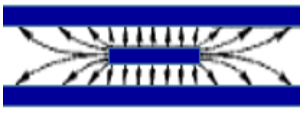
- Microstrip: Quasi-TEM mode
  The electromagnetic field propagates in two different dielectrics, the substrate and air, therefore, the dominant mode is called *quasi*-TEM. This mode has also a 0-Hz cutoff frequency, and for most purposes is very similar to the TEM mode, but its characteristic impedance and propagation constant slowly change with increasing frequency.
  E-field representation:



- GCPW: Quasi-TEM mode
  At low frequency, GCPW typically behaves like a microstrip. At high frequency, slot modes appears
  E-field representation:



- Stripline: TEM mode
  Similar to the coaxial mode as the trace is encapsulated between two conductive plates. Although the transition through the signal via must be carefully optimized.
  E-field representation:



The connector footprint must optimize the signal transmission at the transition to the board and avoid any unwanted reflection or resonances which would limit the electrical performance.

Connector performance

RF board connectors are a little tricky to specify, as the electrical performance strongly depends on the footprint and its associated PCB configuration. Vendors, though, publish standard performance levels for their board connectors. However, it is important to understand that such performance (i.e RL, IL,crosstalk ..) are only valid for a specific footprint and its related board configuration. Any changes in the stackup including dielectric material (Dk, TanD), substrate thickness and metallization thickness can have a significant impact on the final performance of the RF board connector.

For example, we will use the HUBER+SUHNER multicoax connector MXP50 to demonstrate how important the connector footprint is to maximize the electrical performance.

Catalog performance: 1x8A_81_MXP-S50-0-3 (up to 50GHz) (Datasheet)

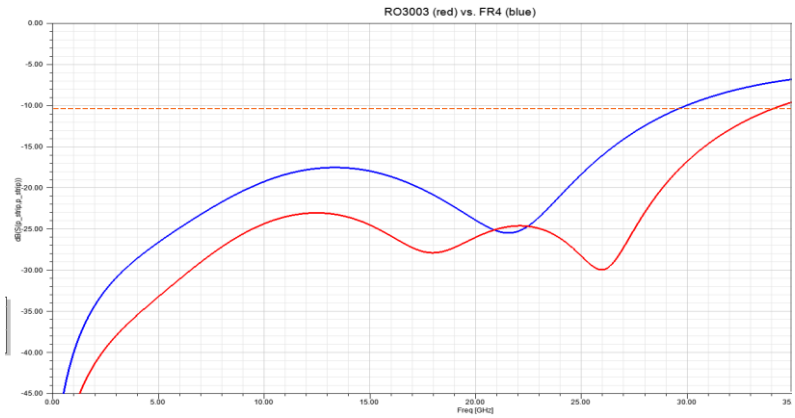
Typical electrical data	Testing condition	Performance
Operating range/data rate		up to 50 Gbps
Frequency range		DC to 50 GHz
Impedance		50 Ω
Return loss	mated condition gated measurement: cable connector/ PCB transition PCB Rogers RO3003 cable: HUBER+SUHNER Multiflex 53-02	≥ 20 dB up to 22.5 GHz ≥ 15 dB up to 50 GHz

Specifications show that excellent RL performance can be achieved with this connector when installed onto a PCB.

Board Stackup

To demonstrate the impact of a board stackup on the performance of a board connector, a simple experiment has been conducted. Simulation A was run on a footprint optimized for microstrip on a RO3003 (5 mil) single layer board. A second simulation, B, was then run after changing the board material from RO3003 to FR4. The trace width was adapted to the new Dk to maintain a 50ohm transition. As graph 3 shows, changing the board material does significantly impact the return loss (S11, S22) performance – in this example over 5dB degradation can be observed. The higher reflection level leads to smaller bandwidth depending on the minimum return loss level one system can tolerate. Should a system targets a return loss better than 10dB then, in this case, the bandwidth will be reduced to 30GHz as opposed to the 35GHz targeted.

Additionally, in the case of an FR4 substrate, the insertion loss is significantly higher. The higher dielectric constant (Dk) of FR4 leads to narrower trace width, generating higher losses.



Graph 3: Simulated S11 results (up to 35GHz): Simulation A (RO3003) in red. Simulation B (FR4) in blue.

Therefore, changing PCB material and/or thickness should be taken into consideration when implementing the connector footprint as it impacts key parameters such as bandwidth, return loss and impedance matching.

Connector footprint: impact on performance

It is often tempting to short cut the footprint optimization process and "recycle" a previous layout to save time during the design phase. However, not taking care of the connector footprint may have disastrous consequences on the test setup and may require an additional and costly design loop.

Let's dive deeper with a more thorough footprint vs performance comparison conducted on the following board configuration:

Routing: grounded coplanar waveguide (GCPW)

Connector: 1x8A_81_MXP-S50-0-3 (up to 50GHz) (Datasheet)

Stackup:

Layer Number	Material	Layer Type	Thickness
1	Copper	Signal	0.82mil
	RO4350B (Dk = 3.66)	Core	9.8mil
2	Copper	GND Plane	0.6mil
	FR4 (Dk=3.48)	Prepreg	20mil
3	Copper	Signal	0.6mil
	FR4 (Dk=3.48)	Core	10mil
4	Copper	Signal	0.6mil

Table 4: Board configuration

Note: Simulation ran with ANSYS Electromagnetics Suite Release 19.1.0.

Most applications today use multilayered boards with core layer thicknesses averaging between 5 and 10mil. So this PCB can be considered representative.

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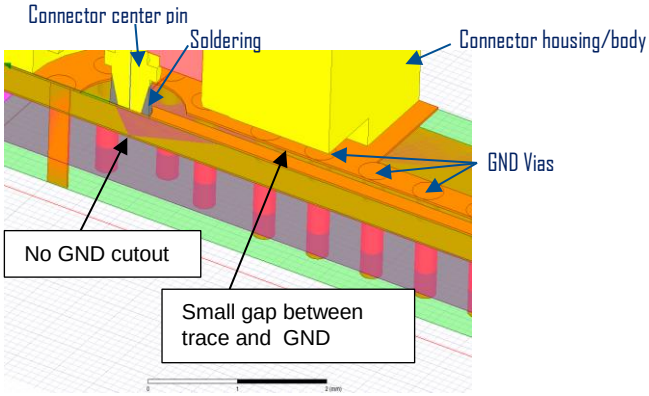
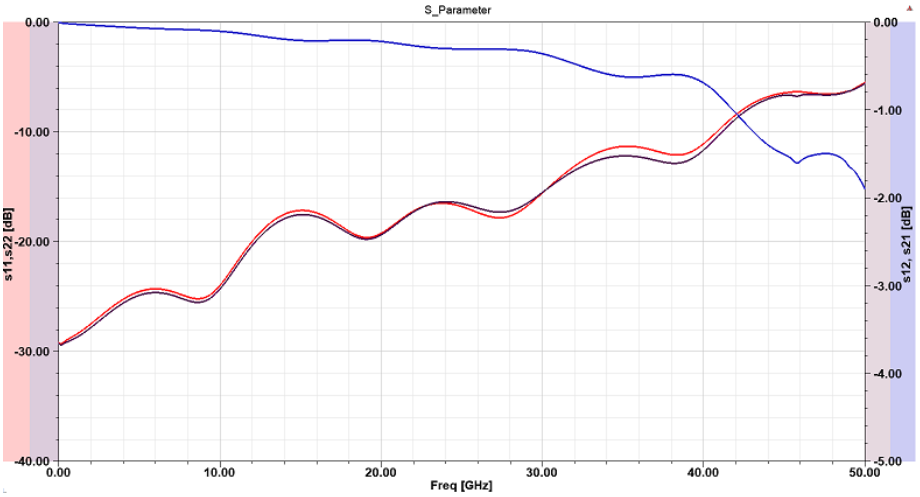
Based on the board stackup shown in table 4, we did simulate two footprints: C (non-optimized) and D (optimized).
Footprint C was simulated using no ground cutout on L2 and using a small gap between the transmission line and its ground on L1.



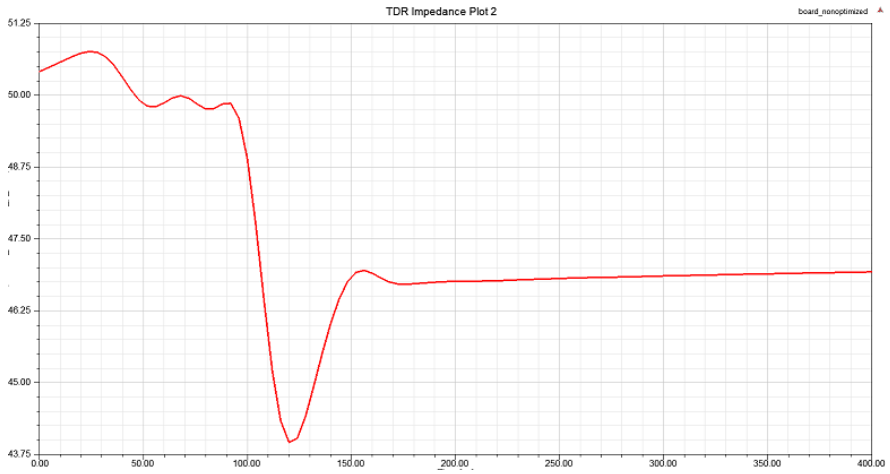
Graph 5: Footprint C design (non-optimzed)

The EM simulations show good performance up to about 30GHz but performance degrades rapidly beyond 40GHz. Return loss falls under 10dB and insertion loss drops drastically beyond 40GHz down to 1.9dB (note that 4.5mm trace included). This simulation clearly reveals the connector bandwidth being reduced to about 40GHz as opposed to the 50GHz originally targeted.



Graph 6: Simulated S-parameters of footprint C (non-optimized).

Time domain reflectometry (TDR) reveals, as well, a large impedance mismatching and a highly capacitive transition to the PCB, explaining the poor S-parameter performance in the upper frequency range. Although the mismatching of the RF connector is often considerably better than the complete system (i.e IC socket & packaging), a 7ohm mismatch for such a transition is not desirable.



Graph 7:: Simulated TDR of footprint C (non-optimized) – Rise time = 20ns.

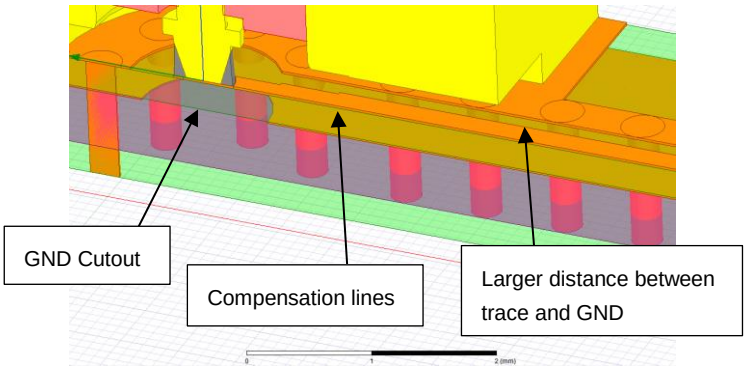
What is, then, degrading the performance?
The high capacitance of this coaxial to planar transition is caused by three major factors. First, the 90degree change in the propagation direction as the signal comes from a vertical mount connector to a board trace. Second, the proximity of the ground plane (L2) to the signal pad (L1) is generating resonance in the upper frequency range, creating a capacitive effect. An additional capacitance is being created by the small air gap between the coplanar waveguide trace and its ground (L1). All these effects degrade the impedance matching as well as the signal transmission at the transition point (connector to board).

In order to maximize the performance of a board connector, HUBER+SUHNER recommends optimizing the connector footprint to match the specifics of each board configuration and provide the full connector bandwidth, enhanced return loss and insertion loss levels as well as an excellent impedance matching.
In order to compensate for the capacitive effects of this stackup, some optimization factors have been implemented into footprint D (optimized):

- GND plane (L2) to SIG pad (L1):
  The minimum size of the signal pad to ensure proper electrical stability and mechanical robustness is given by the size of the connector center pin, the positioning tolerances, as well as solderability. With today's boards often using sub 10mil layers, reducing the size of the signal pad does not suffice. In this case, a ground cutout (L2) is implemented underneath the signal pad. The cutout creates slightly higher losses at lower frequency range but the improvement in the upper frequency band is significant. Special care must be taken in designing this cutout to ensure no parallel modes occur within the stackup. This cutout, when properly designed, has a minimal impact on crosstalk performance.

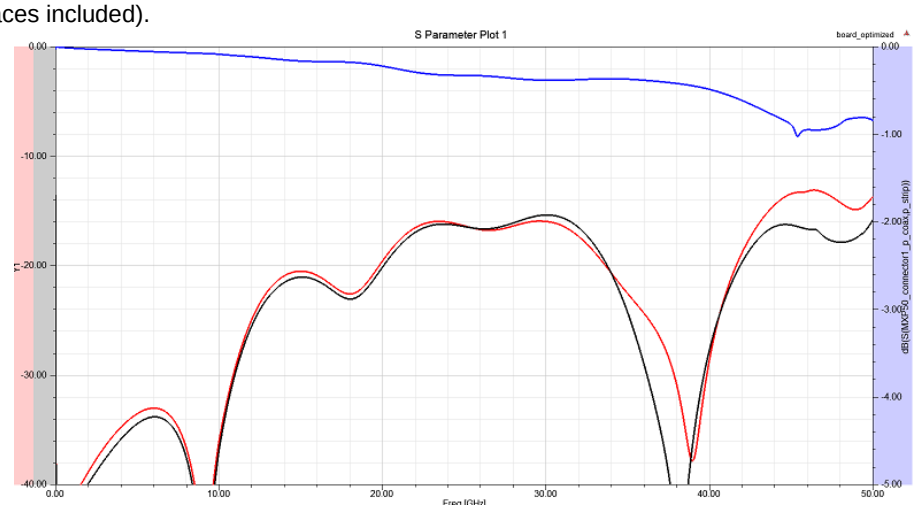
- Air gap between CPW trace and ground (L1):
  Implementing a larger distance between the transmission line and its ground on L1 will reduce the capacitive coupling.

Additionally, a compensation line (L1) was designed in to better the impedance matching and improve the signal transfer from the signal pad onto the GCPW trace. It is common to design the PCB traces with slightly lower impedance (typ. 46-48ohms) to minimize the losses but also because the etching process during PCB manufacturing tends to reduce the line width which increases the impedance. This creates an additional mismatch with RF board connectors, that one typically designed with a 50ohm nominal impedance. The compensation line provides a gradual impedance transition providing better insertion loss and minimizing the capacitive effect.



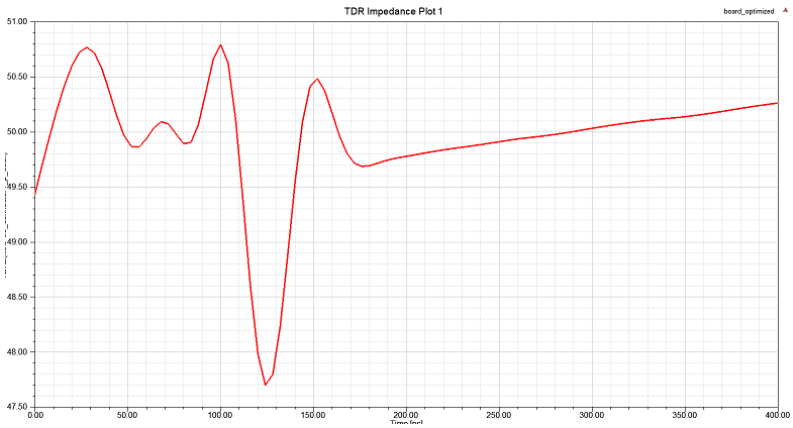
Graph 8: Footprint D design (optimized)

This footprint optimization clearly improves the performance of the connector as shown in graphs 9-10. The full connector 50GHz bandwidth is achieved with return loss better than 13dB across all frequencies. Insertion loss remains linear and below the 1dB level (note 4.5mm traces included).



Graph 9: Simulated S-parameters of optimized footprint D (optimized)

The TDR simulation confirms, as well, the significant performance improvement with smaller capacitance at the PCB transition. The impedance matching is now much closer to the ideal 50ohm target and deviates by less than 2.5ohm which is far better than most components in the validation test setup. This greatly improves the performance of the connector for high data rate application.



Graph 10: Simulated TDR of "optimized" footprint D.

Footprint optimization - Our service

At HUBER+SUHNER, we want to ensure our customers reach the best electrical and mechanical performance from our connectors. As shown earlier, while a “generic” footprint can be used in the early stage to place the connectors onto the board and initiate the routing of all channels, it is crucial to optimize the footprint for a board connector. We do offer engineering services to create a connector layout specifically matching your board configuration. Alternatively, should our customer have in-house know-how and capability to perform 3D EM simulations, we offer a 3D simulation models of our connectors. This approach provides design flexibility to our customers. For further questions on our engineering service, please do not hesitate to contact us: info.us@hubersuhner.com.
It is also important to mention that HUBER+SUHNER has longstanding experience in optimizing RF connector footprints. Our simulations have been fine-tuned over the years to provide an excellent correlation with measurement.

Conclusion:

Some changes on the board stackup can seem to be trivial but neglecting to optimize the footprint of the RF connector can have, as shown above, significant impact on the electrical performance and, ultimately, on the complete test setup. Looking at the total cost of ownership, it is key to validate the footprint to ensure the use of an “electrically transparent” test setup. Also when creating a symbol for an RF board connector in the layout design tool, it is important to mention that an optimized footprint must be generated prior to implementation. Only by using the correct footprint, performance can be maximized!